Suppression of the CPW Leakage in Common Millimeter-Wave Flip-Chip Structures

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***Abstract*— Leakage phenomena in GaAs flip-chip structures, mounted on common GaAs and alumina main substrates, are studied using the spectral domain approach with the goal of reducing possible chip-to-chip crosstalk and transmission resonance. We have found that the TM_0 parallel-plate mode in the main substrate is dominant for the coplanar waveguide flip-chip leakage, and that the leakage can be suppressed by properly selecting the gap height and the main substrate thickness in addition to the dielectric constant.**

***Index Terms*— Flip-chip, leakage, spectral domain approach, TM_0 parallel-plate mode.**

I. Introduction

RECENT advances in integration technology and device performance require higher density packaging of high-frequency integrated circuits. Flip-chip interconnection is emerging as a leading technology to meet the high-frequency and high-density requirements.

The dominant coplanar waveguide (CPW) mode transmission in CPW flip-chip structures, however, becomes leaky above a critical frequency. This leakage travels away from the CPW, and thus results in coupling between multiple chips. The guided power in CPW flip-chip structures leaks in the forms of the transverse magnetic (TM_0) parallel plate mode and the TM_0 surface wave mode [1], [2]. The CPW insertion loss, however, comes mainly from the conductor loss [3], which can be calculated by the phenomenological equivalence method (PEM) [4].

The slight CPW leakage, however, results in serious crosstalk between neighboring circuits and resonance in the transmission due to multiple reflections at finite substrate walls. Thus, the leakage generation criteria should be accurately determined and also suppressed by proper selection and design of the main substrate. T. Krems *et al.* analyzed flip-chip mounting on a quartz ($\varepsilon_r = 3.8$) main substrate [3] and showed that the TM_0 surface wave mode in the chip substrate is dominant for the CPW leakage. This leakage can be suppressed by thinning the chip substrate. As shown in Fig. 1(a), however, the TM_0 parallel-plate mode between the CPW conductor of the chip and the conducting backside of the main substrate is rather important for the chip-to-chip crosstalk in commonly used main substrates of high dielectric constants, such as GaAs ($\varepsilon_r = 12.9$) and alumina ($\varepsilon_r = 9.6$).

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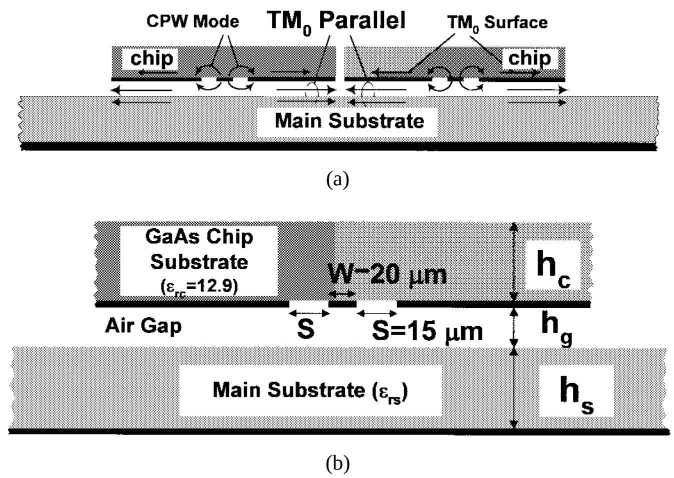


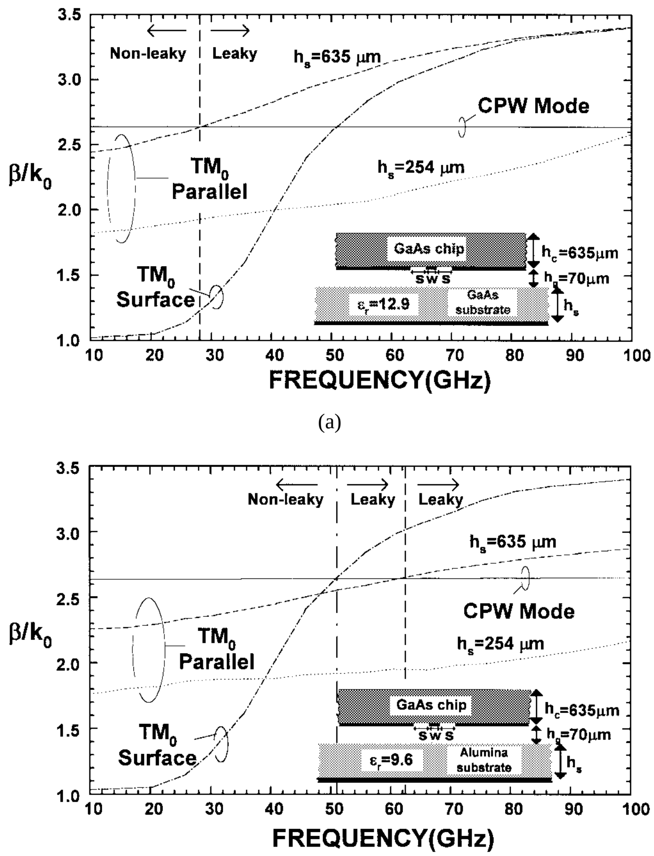
Fig. 1. Schematics of (a) crosstalk to neighboring circuits by TM_0 parallel-plate mode and (b) GaAs CPW flip-chip mounted on a common substrate.

In this letter, we have studied the leakage phenomena in GaAs flip-chip structures on GaAs and alumina main substrates using the spectral domain approach. We have found that the TM_0 parallel-plate mode in the main substrates is dominant for the CPW flip-chip leakage, and that the leakage can be suppressed by properly selecting the gap height and the main substrate thickness in addition to the dielectric constant.

II. Analysis and Numerical Results

Fig. 1(b) shows the cross-sectional geometry of a common CPW flip-chip structure on GaAs and alumina main substrates. The GaAs CPW chip substrate is not conductor backed, but the main substrate is conductor backed for packaging. The propagation constants are obtained using the spectral domain approach (SDA) to take into account the effect of the main substrate [5]. The SDA assumes that the CPW flip-chip is lossless and infinite in length and very wide in width. The discontinuity effect at metal bumps is not considered as well, because our concern is the leakage phenomena within the uniform CPW region far from the metal bumps. The relevant parallel-plate and surface wave modes are analyzed by the analytic equations [6].

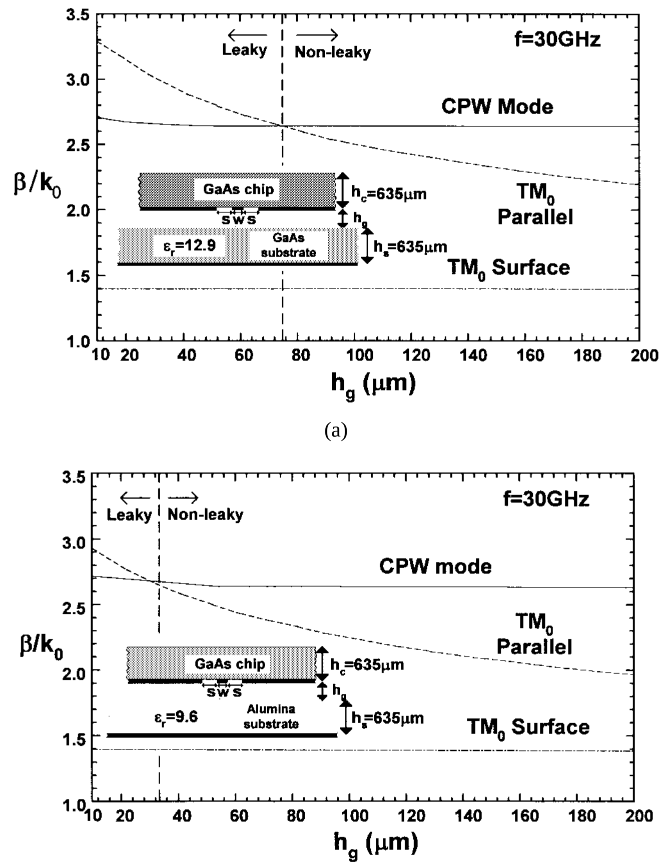
The normalized phase constants of the dominant CPW mode, the TM_0 parallel-plate mode in the main substrate, and the TM_0 surface wave mode in the chip substrate are calculated for GaAs ($\varepsilon_r = 12.9$) and alumina ($\varepsilon_r = 9.6$) main



(a)

(b)

Fig. 2. Normalized phase constants of the GaAs CPW flip-chip mounted on thick ($h_s = 635$ μm) and thin ($h_s = 254$ μm): (a) GaAs and (b) alumina main substrates.



(a)

(b)

Fig. 3. Normalized phase constant variations to the gap height (h_g) for (a) GaAs and (b) alumina main substrates.

substrates with different thicknesses ($h_s = 635, 254$ μm), as shown in Fig. 2. The dominant CPW mode shows a negligible dispersion due to the small CPW dimensions (w, s) compared to the gap height (h_g) and the substrate thicknesses (h_c, h_s). However, the TM_0 parallel-plate mode and TM_0 surface wave mode are strongly dispersive and their phase constants increase rapidly with the frequency [7]. In the case of the thick ($h_s = 635$ μm) main substrate, the phase constants of the CPW and the TM_0 parallel-plate modes coincide at 28 GHz, as shown in Fig. 2(a). Above this critical frequency, the CPW mode becomes leaky, with the leakage in the form of the TM_0 parallel-plate mode. However, the critical frequency increases beyond 100 GHz for the thin ($h_s = 254$ μm) main substrate due to the reduced effective dielectric constant of the TM_0 parallel-plate mode. On the other hand, the critical leakage frequency for alumina main substrates is much higher than that for GaAs main substrates as shown in Fig. 2(b). That is because the effective dielectric constant of the TM_0 parallel-plate mode is proportional to the permittivity and the structural filling factor of the main substrate between the CPW and the conducting backside. Thus, the TM_0 surface wave mode dominates the CPW leakage only for thin and low dielectric constant main substrates such as the thin ($h_s = 127$ μm) quartz ($\varepsilon_r = 3.8$) main substrate examined in [3].

The normalized phase constant variations to the gap height, shown in Fig. 3, are calculated at 30 GHz for different main substrates. The phase constant of the TM_0 parallel-plate mode decreases with the gap height faster than that of the CPW mode. Thus, the CPW leakage can be effectively suppressed by appropriately increasing the gap height. The alumina main substrate has much lower limit of the nonleaky gap height, and hence, has a smaller parasitic inductance of metal bumps for the flip-chip interconnection.

III. Conclusions

Leakage phenomena in flip-chip structures on common GaAs and alumina main substrates are studied, using the SDA, for reducing the possible chip-to-chip crosstalk and transmission resonance. The simulation results show that the TM_0 parallel-plate mode in the main substrate is dominant for the CPW flip-chip leakage, and the leakage can be effectively suppressed by properly selecting the gap height and the main substrate thickness in addition to the dielectric constant.

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